HIGH DYNAMIC RANGE VARIABLE GAIN AMPLIFIER FOR CDMA APPLICATIONS

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ABSTRACT

A new attenuator and threshold voltage (Vth) compensation circuits using GaAs MESFET were designed and developed and this circuit was applied to develop a variable gain amplifier (VGA) for CDMA cellular phone systems. This VGA is packaged in an 8pin plastic package and demonstrated high dynamic variable gain range (80dB/100MHz 70dB/250MHz 55dB/500MHz). High gain of 60dB is observed for 85MHz with low power consumption (Vdd=+2.7V, Idd=6mA). Since depletion mode MESFETs are used no negative supply is needed for gain control.

INTRODUCTION

CDMA cellular phone systems require accurate wide dynamic range power control. Low price and high efficiency are also needed to make CDMA more popular as a cellular phone solution. To achieve this wide dynamic range VGA using 0.5μm gate length GaAs MESFETs are developed. GaAs FET is suitable to high frequency, low voltage and low power applications such as mobile communication systems. However GaAs FETs are seldom used for analog ICs applications where large variation in Vth and negative gate bias are required. Newly developed VGA circuit suppress this large variation and operates without a negative voltage.

CIRCUIT DESIGN

Figure 1(A) shows a basic schematic diagram of the MMIC VGA. This MMIC consists of common source amplifiers and attenuators. FET Q2 operates as a variable resistor. DC voltage between the source and the drain is equal to 0 V. Input signal is amplified to Q1 and is split between R3 and Q2.
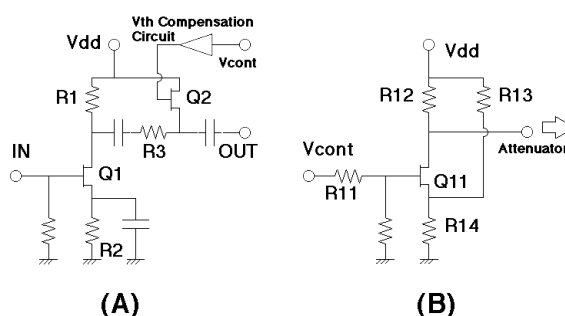

Figure 1: Block diagram of basic configuration (A) and Vth condensation circuit (B) for VGA.

Since the change of gate or drain bias condition is not required for gain control in the gain stage, the developed VGA has lower distortion than the conventional one. In order to use a positive supply for gain control a depletion mode FET is used along with the power supply node as RF ground. The attenuator circuit is designed so that it dose not consume any current.

It is well known fact that the threshold voltage(Vth) of GaAs FETs has large variation and this affects the attenuation sensitivity for a given control voltage. Figure 1(B) shows the block diagram of the compensation circuit for Vth variation. The gain slope Vs input voltage can be adjusted by R11, R12, R13 and R14. FET Q11 inverts the input voltage. The attenuator and compensation circuits are on a same small chip. It is also well known that for

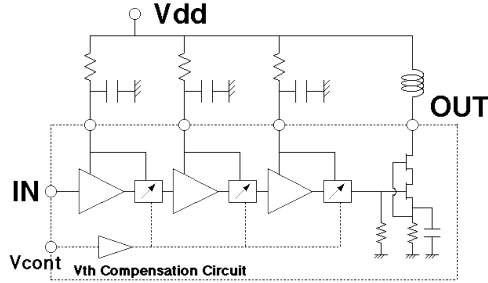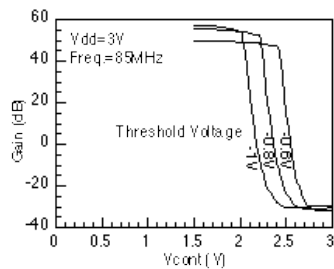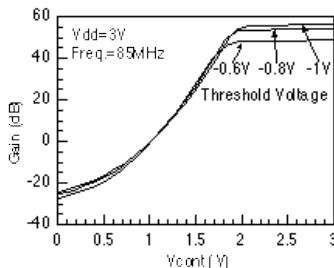a closed GaAs MESFET structure the Vth variation is small.

Figure 2 : Block diagram for the developed VGA and its external circuits.

Figure 2 shows block diagram for the developed VGA and its external circuits. The VGA includes 3 stage amplifiers with attenuator circuit, a Vth compensation circuit and an open drain final stage. Input and output impedance are designed for $10k\Omega$ and grater than $5k\Omega$ respectively. External capacitors for RF ground in each power nodes and RF choke for final stage are required.

Figure 3(A) shows the simulated gain slope variation without compensation circuit and figure 3(B) shows similar data with the compensation circuit for Vth from -0.6V to -1.0V. The typical value is -0.8V. As one can see from figures 4A and 4B, gain slope has large variation without the compensation circuit and there is hardly any variation since the compensation circuit is included.

MANUFACTURING

Figure 4 shows the photograph of the MMIC VGA. Die size is 0.90mm x 0.95mm. The gate length is 0.5μm and ion implanted MESFET processing is used. Low power application requires low knee voltage for reduce the supply voltage and this is obtained by shorted gate GaAs FET [1][2]. Low drain conductance and low leakage current are required for operation under deep gate bias or low current supply. The channel confinement and drain conductance are improved by optimizing the doping concentration and annealing conditions.

Figure 3 : Simulated gain slope of VGA without Vth compensation circuit (A) and with Vth compensation circuit (B).
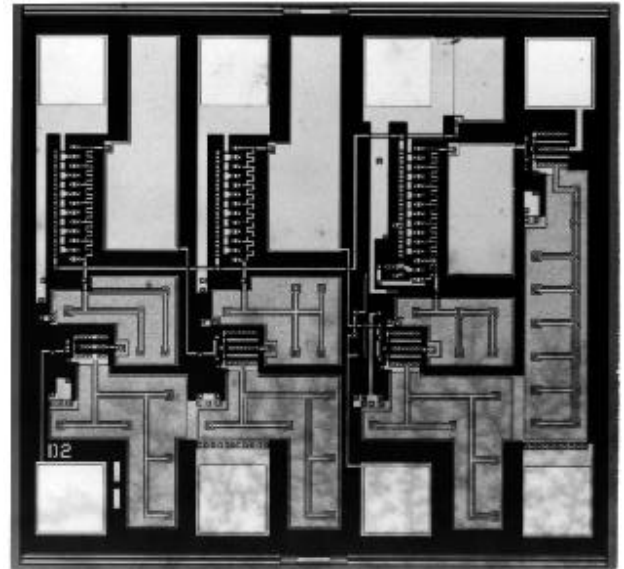

Figure 4 : Photograph of the developed VGA chip.

The MMIC VGA is packaged in an 8 pin plastic package to reduce the cost. The out is kept away from the input to avoid RF feed back. The isolation between output and input was compared for ceramic and plastic package and no difference was found.

TEST RESULTS

Figure 5 shows measured gain slope for the VGA. Upper and lower bounds are indicated by dotted lines and typical curve is drawn by solid line as a statistical data for 50 samples. Input and output were reactivity matched to 50 ohm at 85 MHz. The supply voltage and current are +3V and 6mA respectively. The maximum observed gain as 60 dB and minimum gain as -25 dB. The variable gain range is 85 dB. The variation of gain slope is considered that is due to crystal imperfection in microscopic area [3].

Figure 6 shows the frequency response for maximum and minimum gain. For this measurement no external matching circuit was used. The maximum variable gain achieved at 100 MHz is 80 dB. As the operating frequency is increased it was observed the maximum gain decreases and the minimum gain value increases. The variable gain range is 70 dB at 250 MHz and 55 dB at 500 MHz.

Figure 7 shows gain as a function of supply voltage. Change of maximum gain is hardly seen in the high voltage region (Vdd>2.6V). The VGA can be driven by single cell of Lithium ion battery.

Gain slope is measured over temperature from -30 to +85°C and are shown in figure 8.

8dB of gain difference is seen between Vcont of 0 to 3V. The difference is mainly caused by variation for the resistance on GaAs chip. The resistor is made of doped GaAs substrate and has a temperature coefficient of +0.17%/°C. The gain is determined by R1 and R2 shown in figure 1(A). Higher value of R1 produces larger gain and R2 reduce the gain. R1 and R2 are designed for compensate the gain variation over temperature.
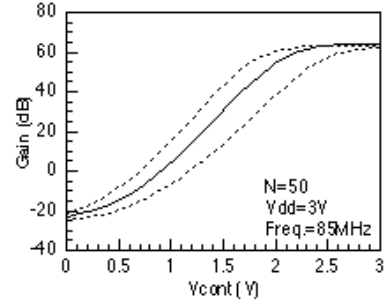

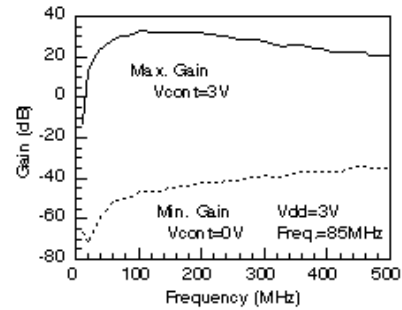Figure 6 : Measured gain slope for theVGA.

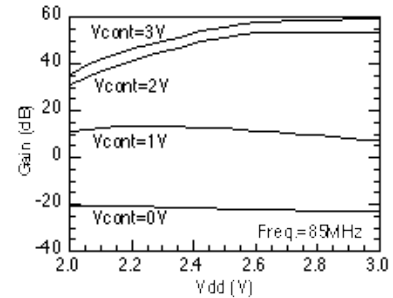Figure 7 : Frequency response for maximum and minimum gain.

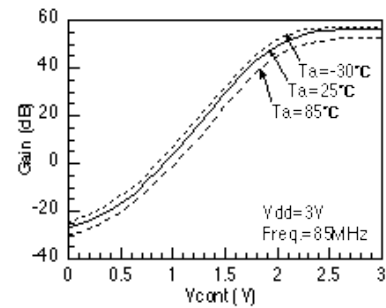Figure 8 : Gain vs. supply voltage.

Figure 9 : Gain slope at temperatures.

CONCLUSION

This newly developed part has greater than 80 dB VGA range for 50-100 MHz and greater than 70 dB range for 100-250 MHz range. The operating conditions are +3V and 6mA. Since depletion mode FETs are used no negative supply is needed for gain control. Gain variation from part to part is controlled using Vth compensation control circuitry. The VGA is a MMIC chip which consists of 4 gain stages, 3 attenuator stages and a Vth compensation circuit stage. This 0.5 µm gate length GaAs MESFET devices is packaged in an 8 pin plastic package. The control voltage is also a positive voltage. Only a few external components are needed. All the above mentioned features make this VGA a highly efficient low cost solution for wide dynamic range applications.

REFERENCES

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